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Wafer Scale Integration of III-Vs (GaN) with Si CMOS for RF Applications

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Outline

- Evolution of Microelectronics
- Why Heterogeneous Integration of Dissimilar Materials?
- Integration of III-Vs with Si CMOS
  - Advanced Multi-chip assemblies
    - Advanced Packaging
    - Chip on wafer/interposer
  - Monolithic Integration
    - InP HBT and Si CMOS
    - GaN and Si CMOS
  - Wafer bonding
    - GaN and Si CMOS
    - GaN on 200 mm Si
- Insertion Opportunities
- Summary

Future Vision: Sensors/Systems on a Chip, But how do we get there?

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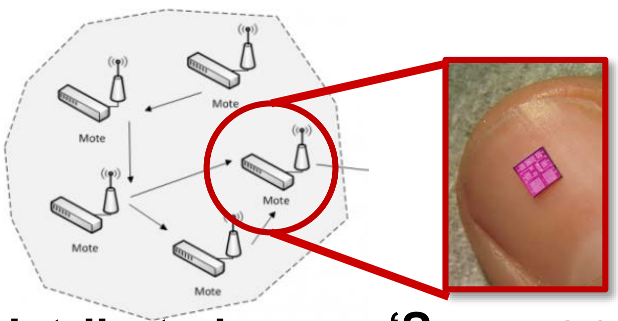
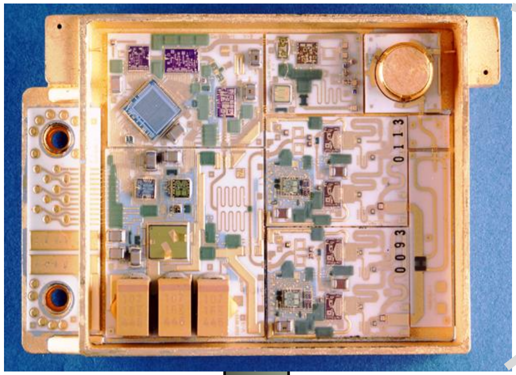
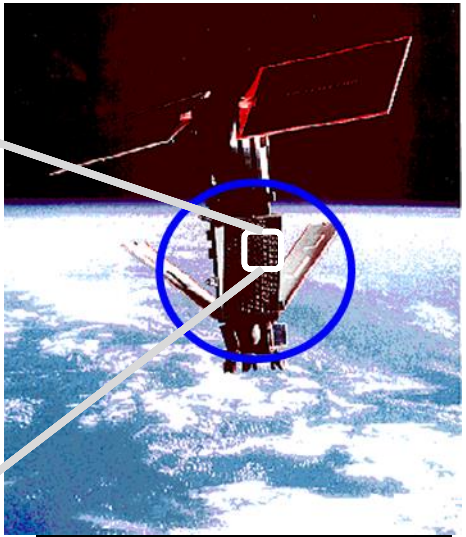


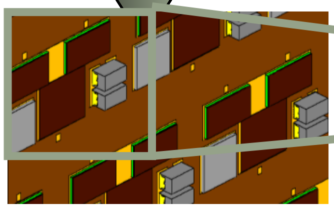
'Distributed Sensor Network'

'Senor-on-a-chip'

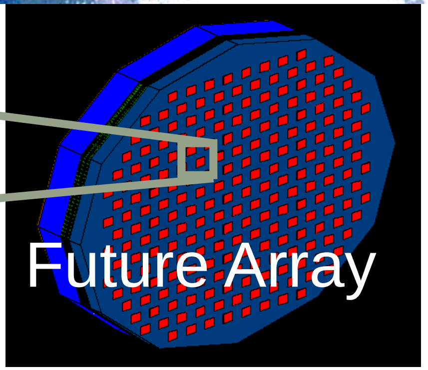
Traditional Multi-chip Module







'Transceiver-on-a-chip'



Higher Integration Offers Path to Enhanced Performance, Lower Size and Cost

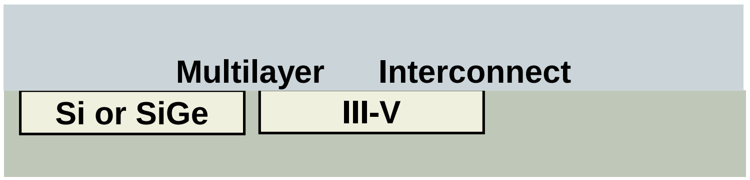
Why Heterogeneous Integration (HI)?

- **Facts:**
  - If it can be done in silicon it will be
  - III-V devices provide superior performance
    - High power, efficiency, frequency, switching speed, dynamic range, linearity ….
- **Can we get best of both worlds?**
- **What is the 'best' way to integrate III-V devices with high density, low cost Si ?**
  - Traditional Hybrid assemblies
  - (Advanced) Multi-chip assemblies
  - Chip-scale Heterogeneous Integration (HI)
  - Monolithic Integration
  - Wafer-scale HI (3DHI)

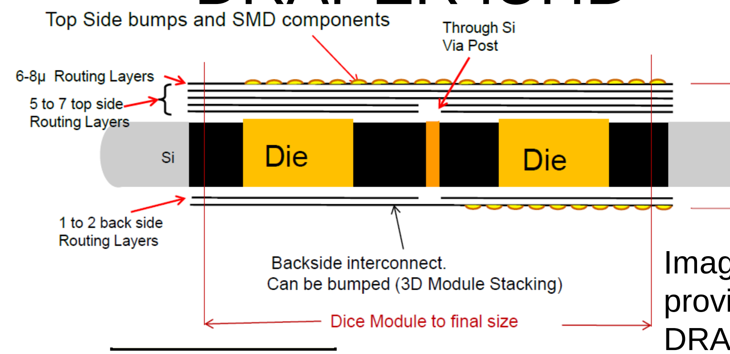
Challenge:
Engineer a cost effective heterogeneous integration solution

Adv. Multichip Assembly (Advanced Packaging)

Individual Die in Adv. Multichip Assembly

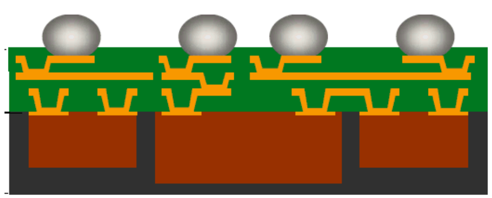


DRAPER iUHD

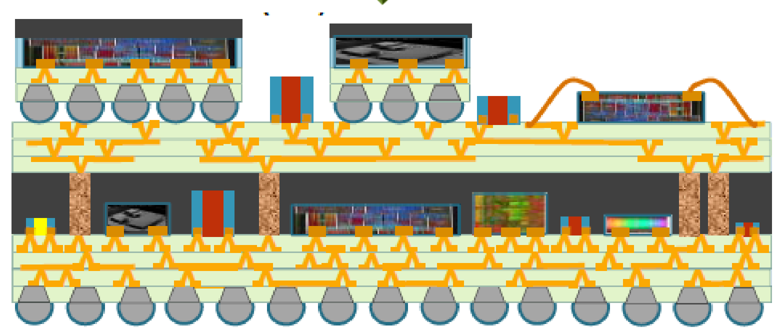


Images provided by DRAPER

Freescale RCP



Images provided by Freescale



Stacked Multichip Assemblies (e.g., RCP on RCP, iUHD on iUHD)

Multi-chip assemblies:
Chip scale Packaging to 2.5/3D Integration

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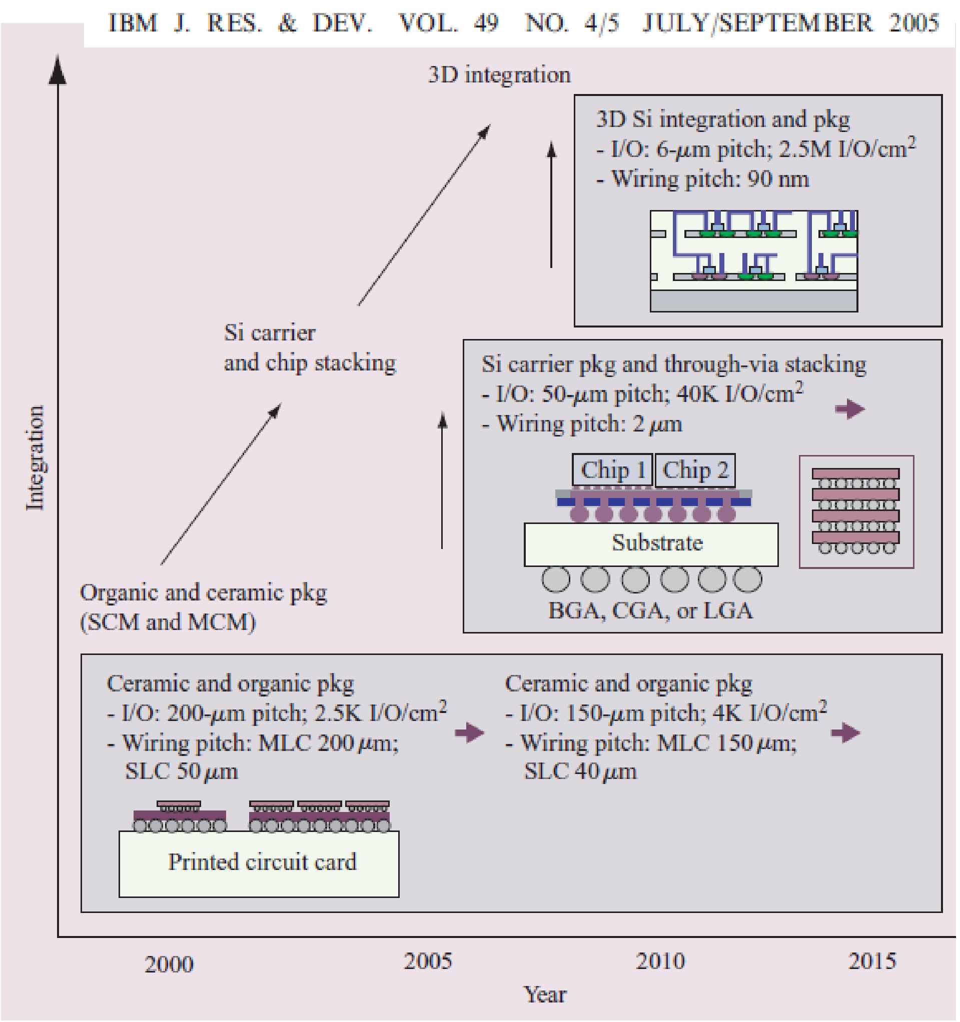
- 2.5D Integration
  - chip on interposer
- 3D Integration
  - Chip Stacking
  - Si-Si wafer bonding
    - IBM, Tezzaron

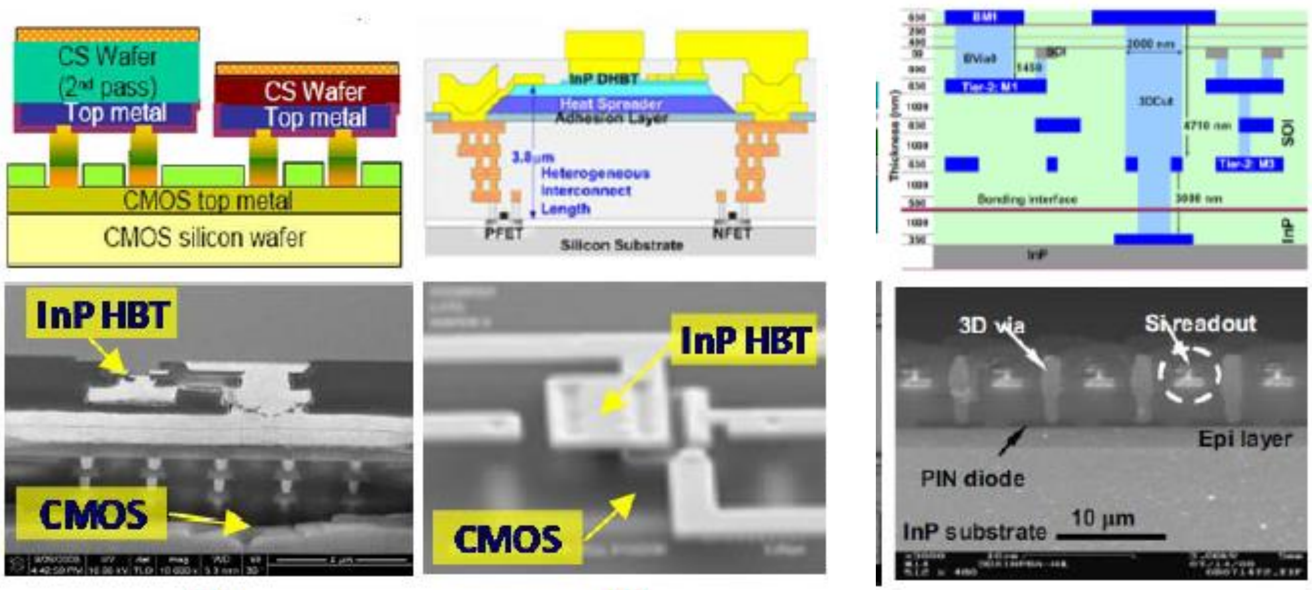
Advanced Packaging Leverages Standard Si Back End Interconnect Processes to Achieve High Level of Integration and Low Cost



Heterogeneous Integration Approaches

- Chip Scale:
  - NGAS (a) – die on wafer
  - HRL (b) – epi transfer
- Wafer Scale:
  - MIT LL (d) – wafer bonding

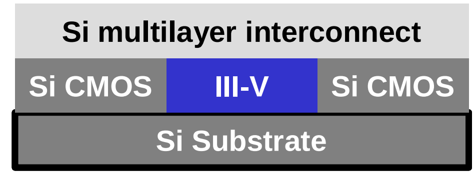
S. Raman S, T.-H. Chang, C.L. Dohrman, M.J. Rosker, "The DARPA COSMOS Program: The Convergence of InP and silicon CMOS Technologies for High-Performance Mixed-Signal," *International Conference on Indium Phosphide and Related Materials*, PL2, (2010).



(a) (b) (d)

Direct Monolithic Integration

- Fabricate III-V devices directly on Silicon wafer
  - Similar to SiGe BiCMOS process
- Advantage
  - Planar process
  - Leverage Silicon IC Fabrication Infrastructure
- Challenges:
  - Minimize impact on standard Si (100) processing
  - No degradation of CMOS performance
  - No degradation of III-V performance
  - Compatibility with high interconnect density
  - Provide cost effective solution
    - Large diameter (200mm, 300mm) wafers
    - Fabrication entirely in a Si foundry
    - Au-free metallurgies



III-V CMOS Integration

III-V devices embedded in a Si wafer using III-V templates and standard Si multilayer interconnects and processing

Direct Monolithic Integration
InP – Si BiCMOS

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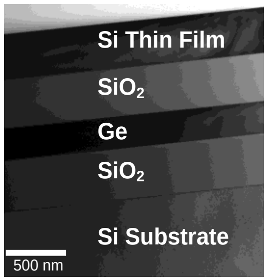
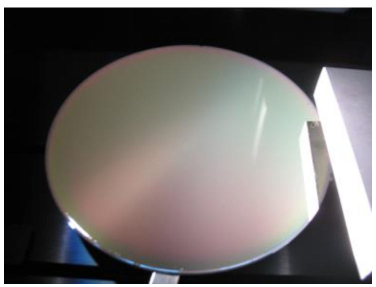
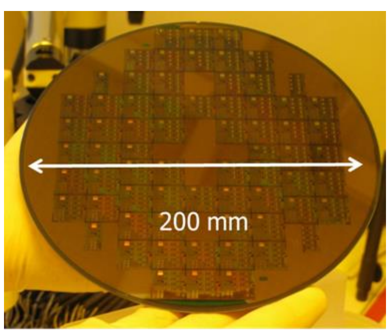
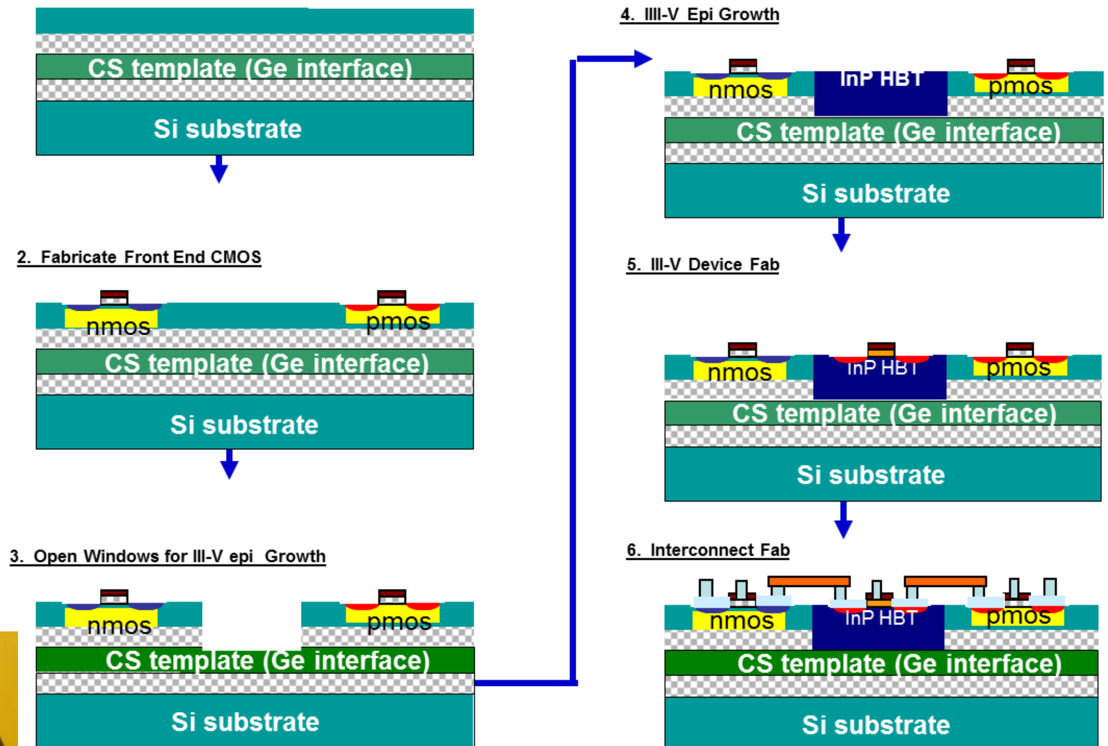
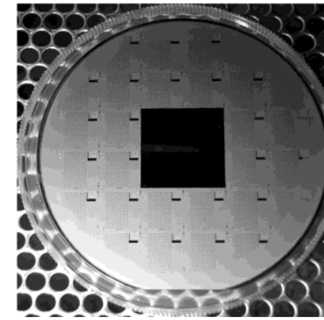


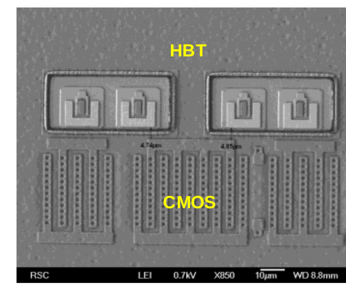


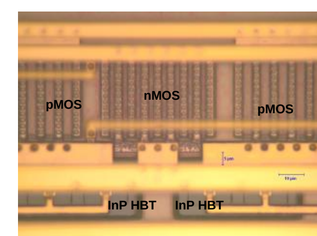


Starting Substrate: Soitec's Silicon On Lattice Engineered Substrate (SOLES)









Integration Process Demonstrated on 100 mm wafers

Direct Monolithic Integration GaN – Si CMOS

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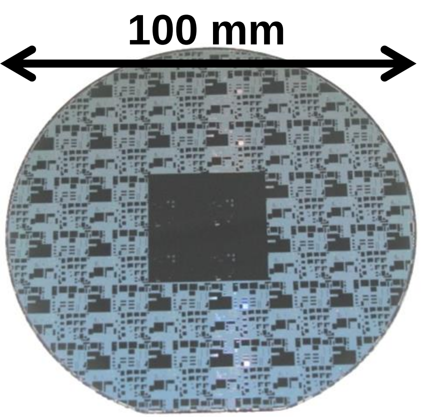
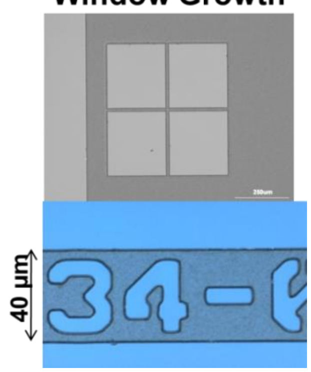
100 mm



Window Growth



Starting Substrate (SOI on Si<111>)

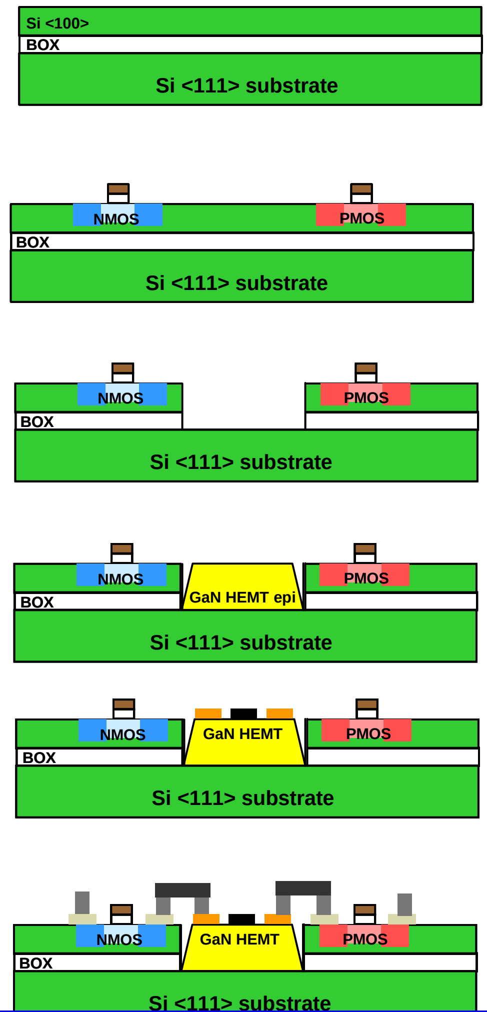
Fabricate CMOS

Etch window To <111> Si

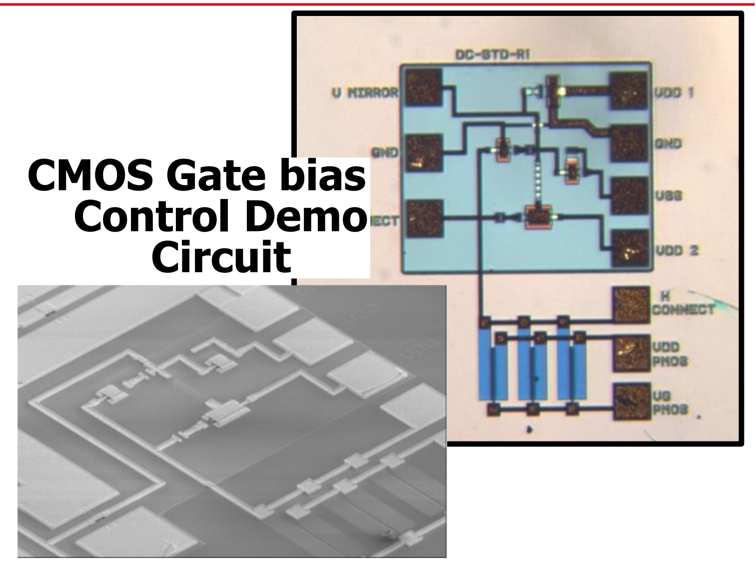
Grow GaN HEMT epi

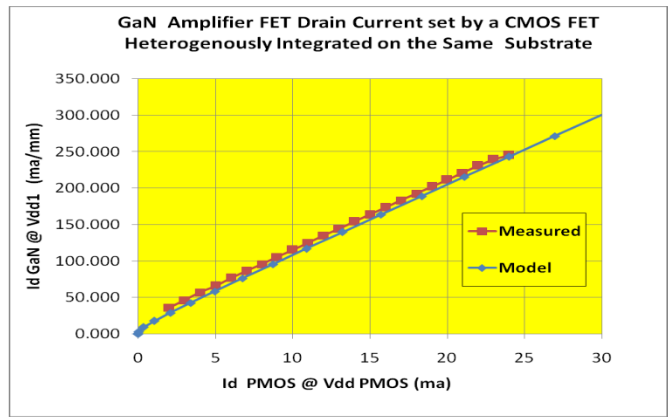
Fabricate GaN HEMT

Heterogeneous Interconnects



CMOS Gate bias Control Demo Circuit





First Demonstration of GaN – Si CMOS Heterogeneously Integrated RFIC

Wafer scale Heterogeneous Integration: Wafer bonding

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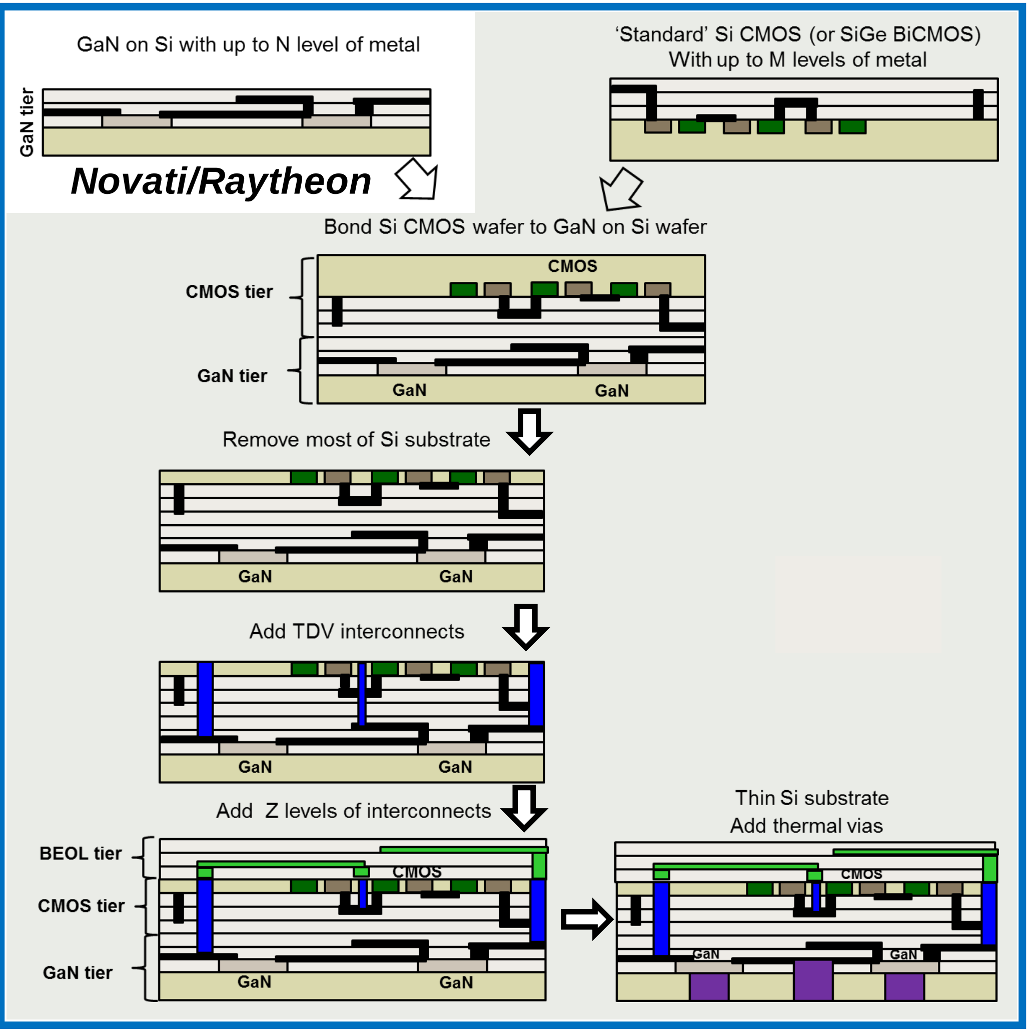


Approach

- Integrate fully processed III-V (GaN) and Si CMOS wafers
- Oxide-oxide wafer bonding
- All 200mm wafers
- All Fabrication in Si Foundries
- Au-free, Si-Like processing (of GaN)
- Cu RF lines, interconnects, Thermal Via
- All Optical lithography (< 50nm capable)
- Semi-Standard 725 µm thick, 200 mm diameter Substrates
- GaN on bottom, close to heatsink

COMPATIBILITY

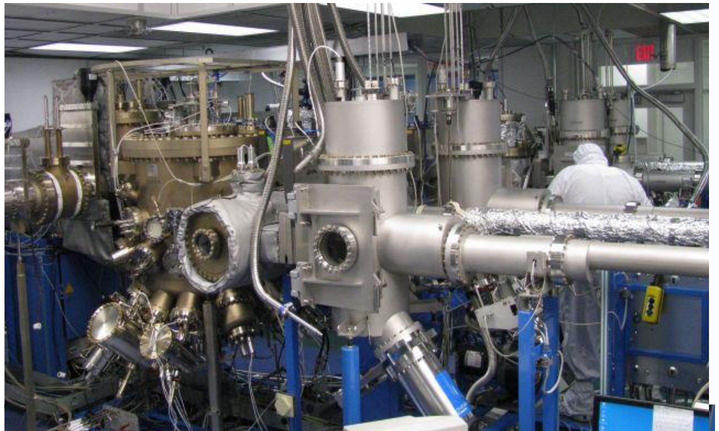
- Any CMOS node, Any SiGe BiCMOS, any foundry
- Any GaN node
- Integrate other active and passive components
  - InP, MEMS, magnetics, etc..
  - Chip-scale
  - Wafer-scale
- Compatible with Advanced Thermal Management Approaches

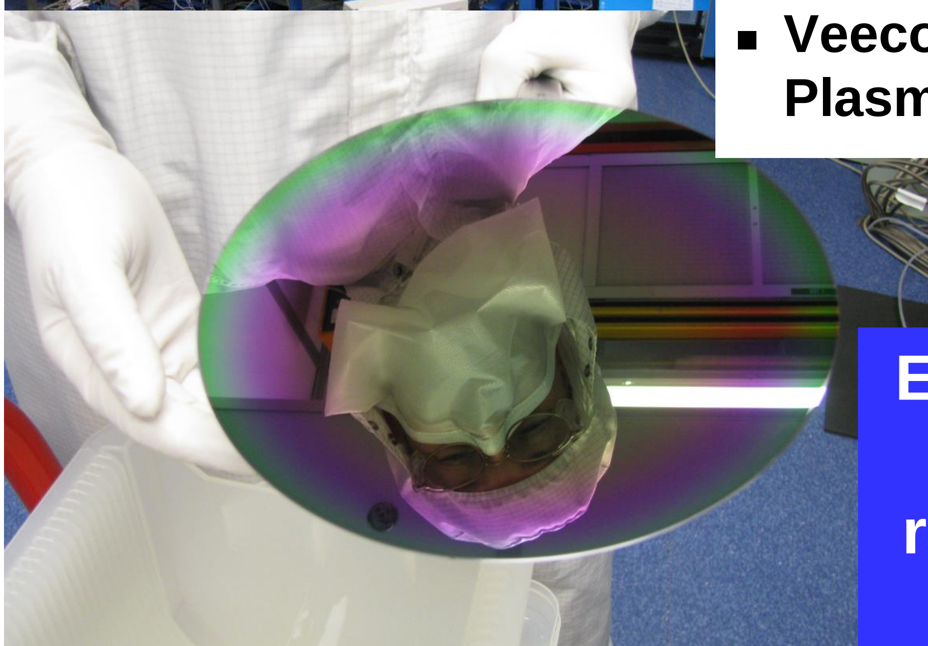
Wafer-scale Heterogeneous Integration:

- How do we get there?
  - – Implement in Si foundry
  - – Scale (III-Vs) GaN on Si to 200 mm
    - Au free metallurgy
  - – Wafer bonding of ‘dissimilar ‘ materials

- Where are we today?

GaN growth by MBE on 200mm Si wafers



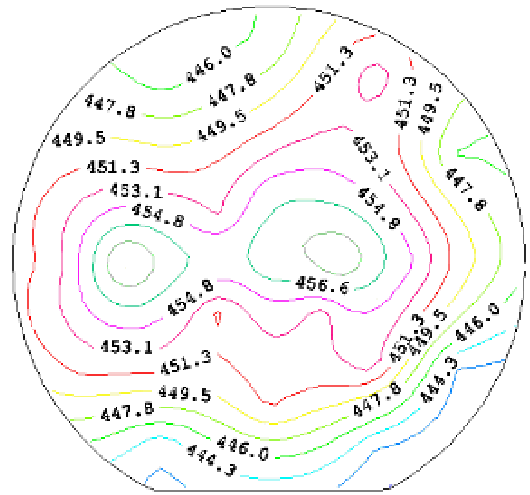


Riber 49NT production MBE machine

- **4x100-mm wafers or 1 x 200-mm wafer**
- **Veeco Nitrogen Plasma Source**

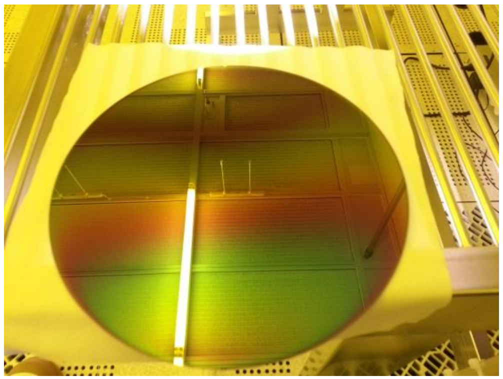
Statistical Summary

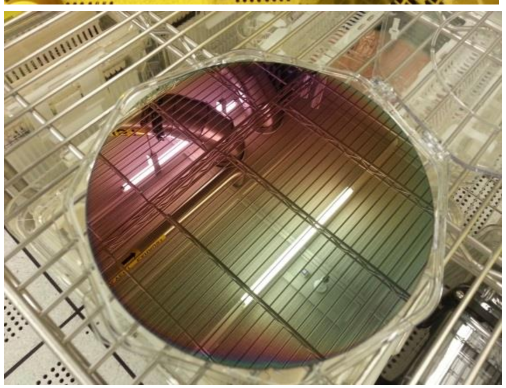
Number of Test Points	29
Average Value	451.4
Maximum Value	460.7
Minimum Value	442.3
Sample Spread(%)	4.08
Std Dev Value	5.0
Wafer Uniformity Value(%)	1.12
Contour Interval Value	1.758



Excellent GaN HEMT transport properties, uniformity and repeatability demonstrated on 200mm wafers by MBE

GaN HEMT epi on 200 mm Si by MOCVD





IQE GaN on <111> Si, 200mm Wafers

- **Semi Standard 725µm thick wafers**

Mobility ~1,600 $cm^2/V\text{-}s$

Delivery	Batch	Number of Wafers	Bow (in microns)			
			Average	Std Dev	Max	Min
1	1	9	18	8	30	8
	2	16	19	7	34	5
2	1	15	14	4	21	8
	2	10	14	10	31	-3

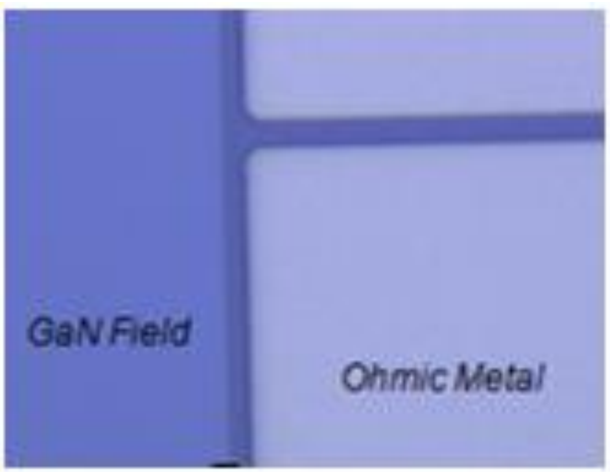
Average Wafer Bow ≤ 25µm

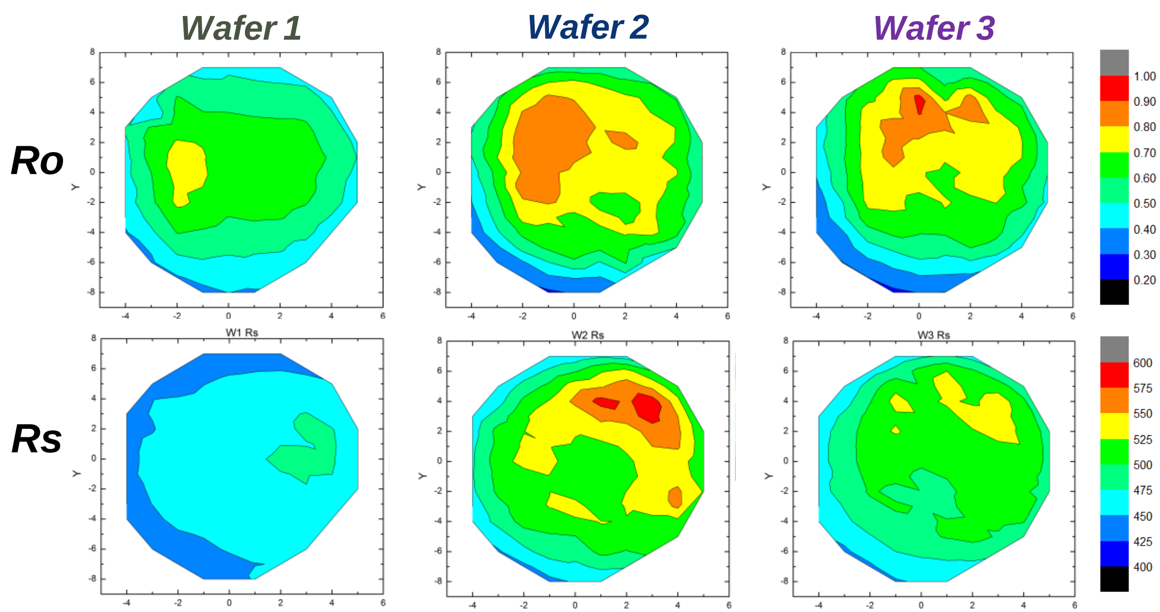
Max Wafer Bow ≤ 35µm

IQE Has Demonstrated Excellent Material and Wafer Bow Characteristics on SEMI Standard <111> Si Wafers

Au-free ohmic contacts to GaN

Type	Ohmic Contact Metallurgy	Contact Resistance, R_o (Ω-mm)
GaN on Si	Au-free	0.354
GaN on SiC	Au-based	0.33





Au free ohmics demonstrated on 200 mm diameter wafers in Si foundry

Cu Damascene GaN on 200 mm Si Integrated MMIC process

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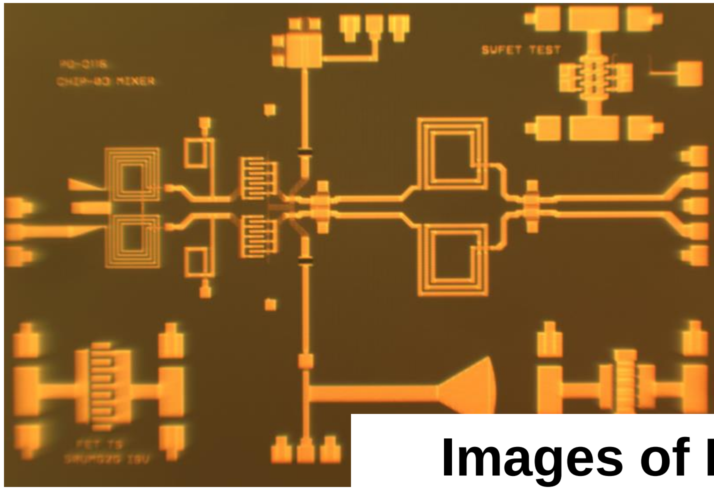
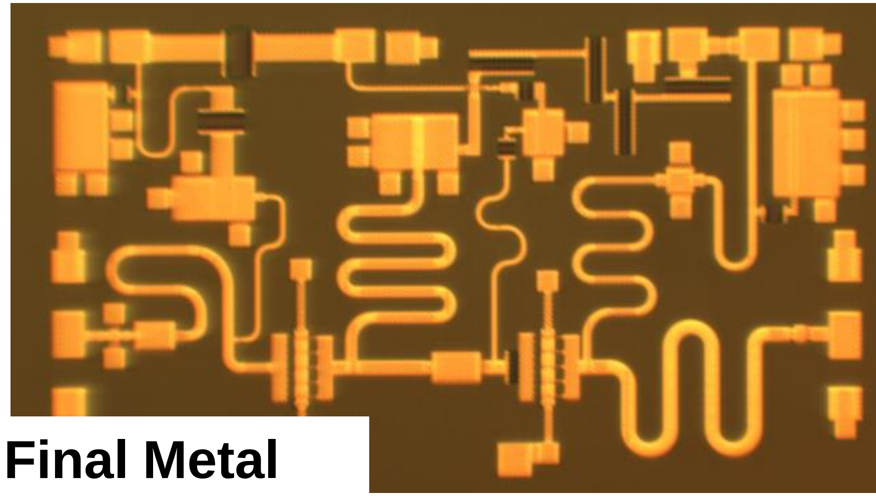
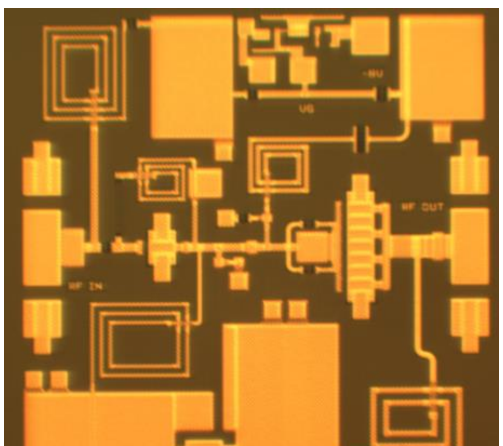
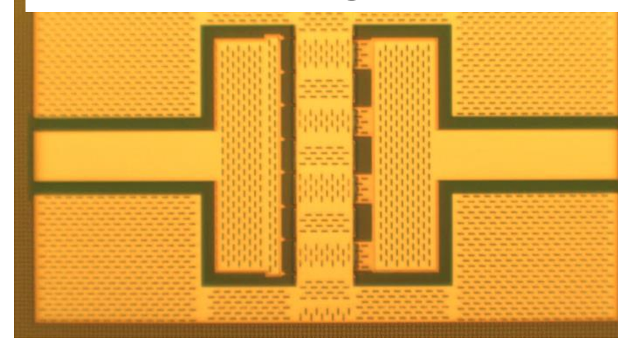




Images of RF ICs at Final Metal



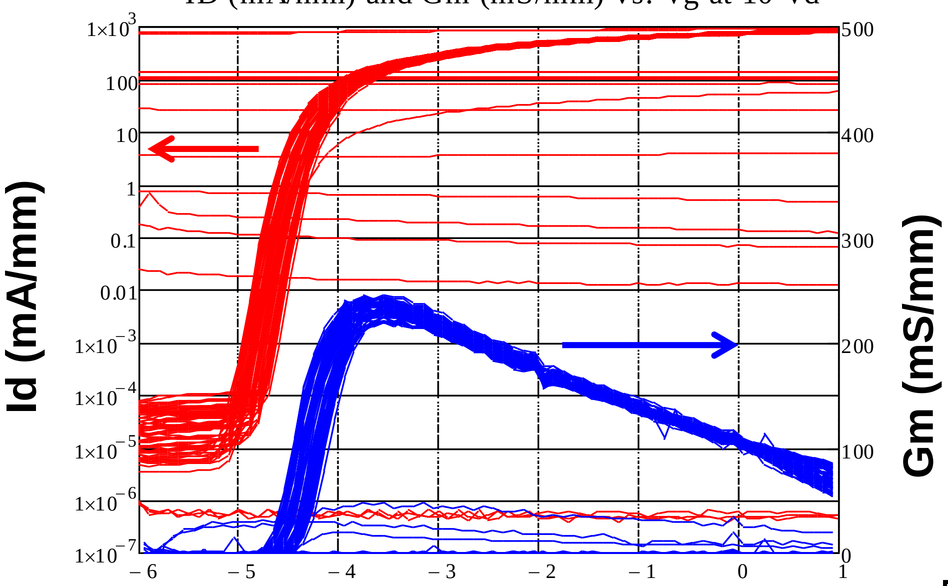
Multi Finger FET

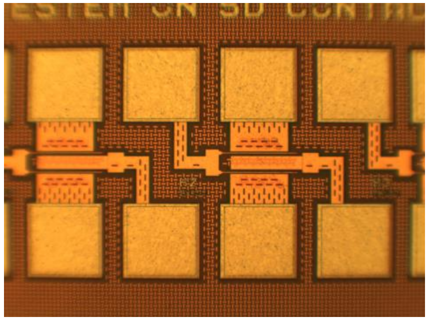


3 levels of Cu Metal Layers, TaN Resistors and MIM Capacitors Successfully Integrated on 200mm GaN on Si Wafers

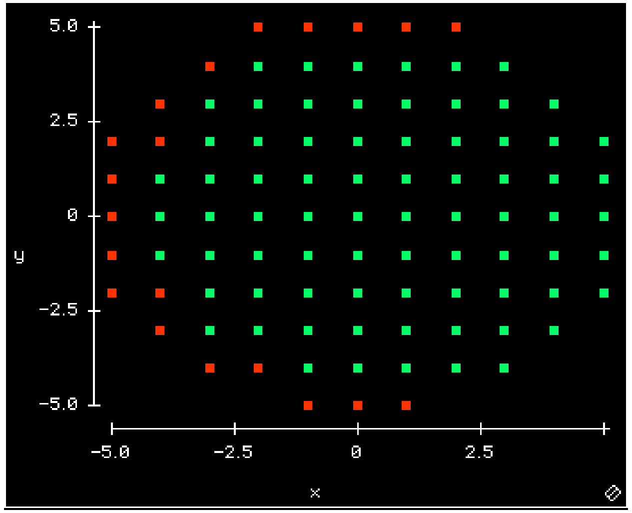
GaN on 200 mm DC Functional Yield

All 95 Reticles, 1x100um Devices





Pass (Green) /Fail (Red) Wafer map (All Device Failures are Edge Die)



DC statistics (excluding edge die)

Variable	Mean	StdDev	Count	Failures	Passing	Yield %
IMIN	2.53E-05	1.45E-05	75	0	75	100
IDSS	784.3	34.3	75	0	75	100
IMAX	876.7	35.6	75	0	75	100
VP	-4.5	0.15	75	0	75	100
Gm Max	239.9	7.5	75	0	75	100
Vg @ Gm	-3.6	0.15	75	0	75	100

100% Post Gate DC Functional Yield

Excellent DC Uniformity and Functional Yield across 200 mm wafer

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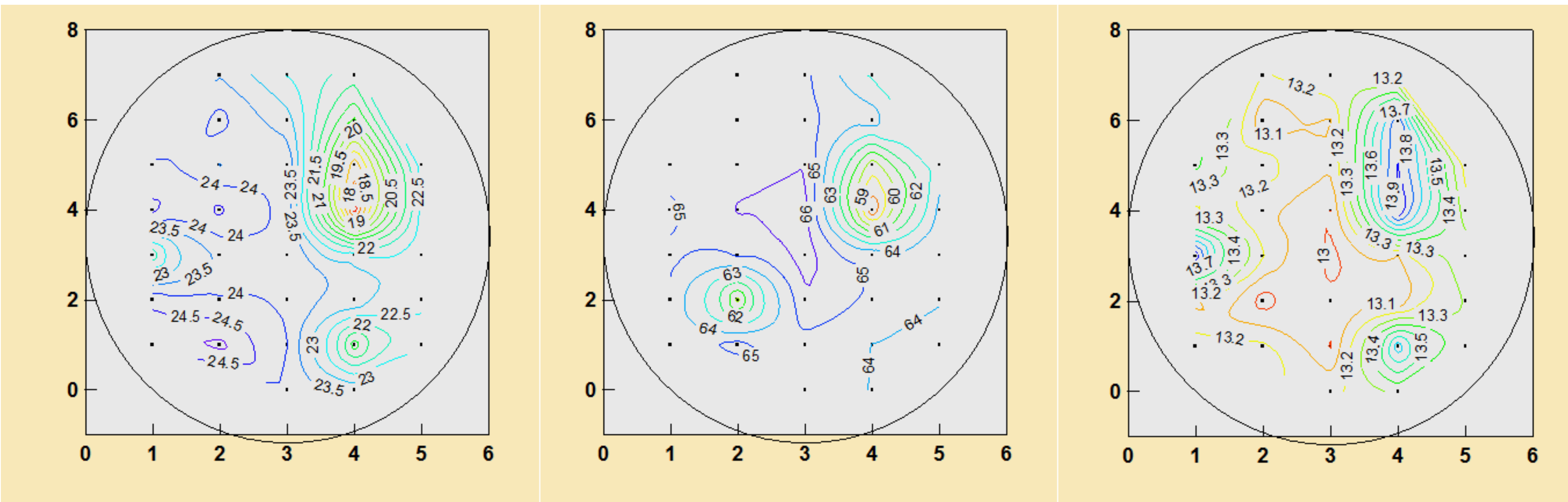
GaN on 200 mm Si
Small single RF Characteristics

f_T [GHz] | f_{MAX} [GHz] | 10 GHz G_{MAX} [dB]



f_T [GHz]	f_{MAX} [GHz]	10GHz G_{MAX} [dB]
23 +/- 2	64 +/- 2	13.3 +/- 0.3

Excellent, uniform, small signal RF characteristics across 200 mm wafer

GaN on 200 mm Si
Pulse I-V Performance

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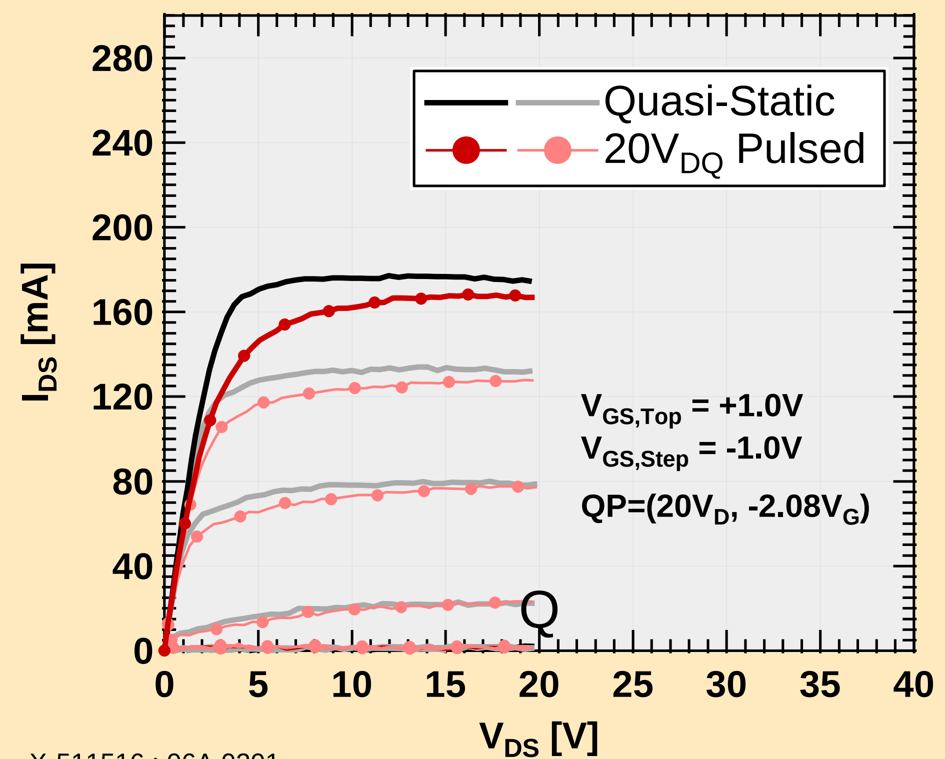
- GaN on 200 mm Si by MBE
- Pulsed I-V measurements on GaN on 200 mm Si wafers exhibit good DC-RF dispersion



X-511516 : 06A.0201

QS-I_{MAX}	QS-R_{ON}	ΔR_{ON}	Dispersion	I_{DLC}
885 (37)	3.19 (0.24)	1.06 (0.74)	20 (11)	6 (2)

GaN on 200 mm Si
CW LS RF Performance (Load Pull)

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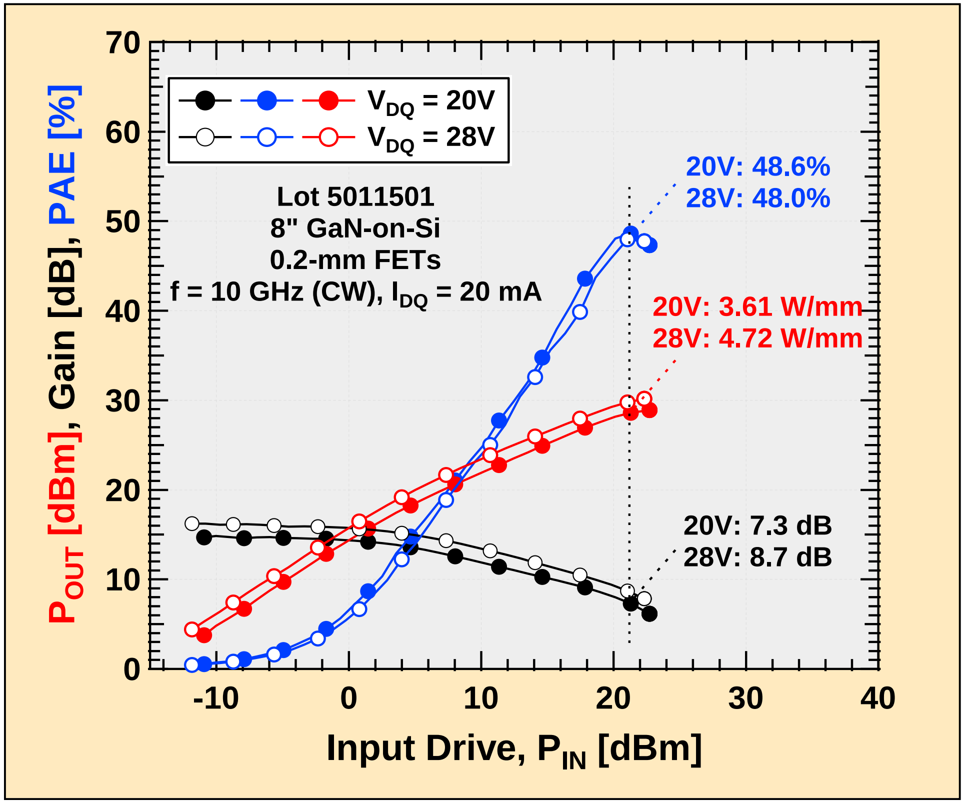
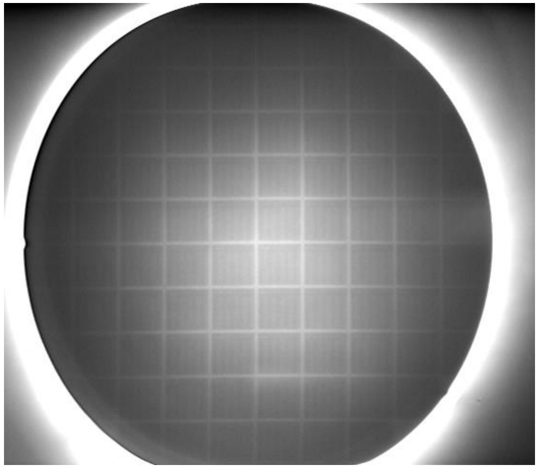


▪ GaN-on-200 mm Si by MBE delivers:

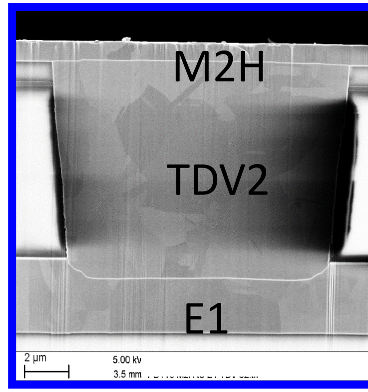
- 3.6 – 4.7 W/mm
- 7-9 dB gain
- 48-49% PAE
- (20-28V)

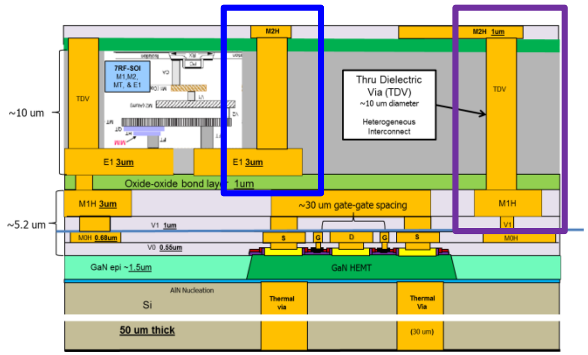
GaN on 200 mm Si RF performance approaching performance of mature GaN on SiC

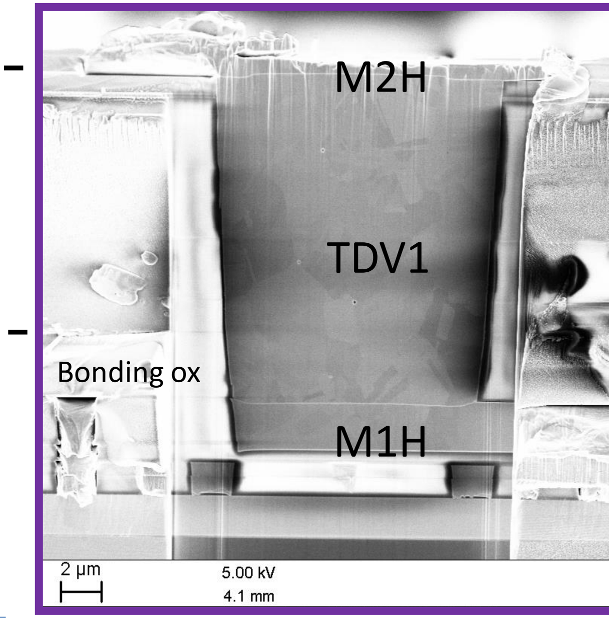
Si CMOS – GaN on Si wafer bonding and heterogeneous interconnects



IR image of metallized bonded 200 mm wafer pair



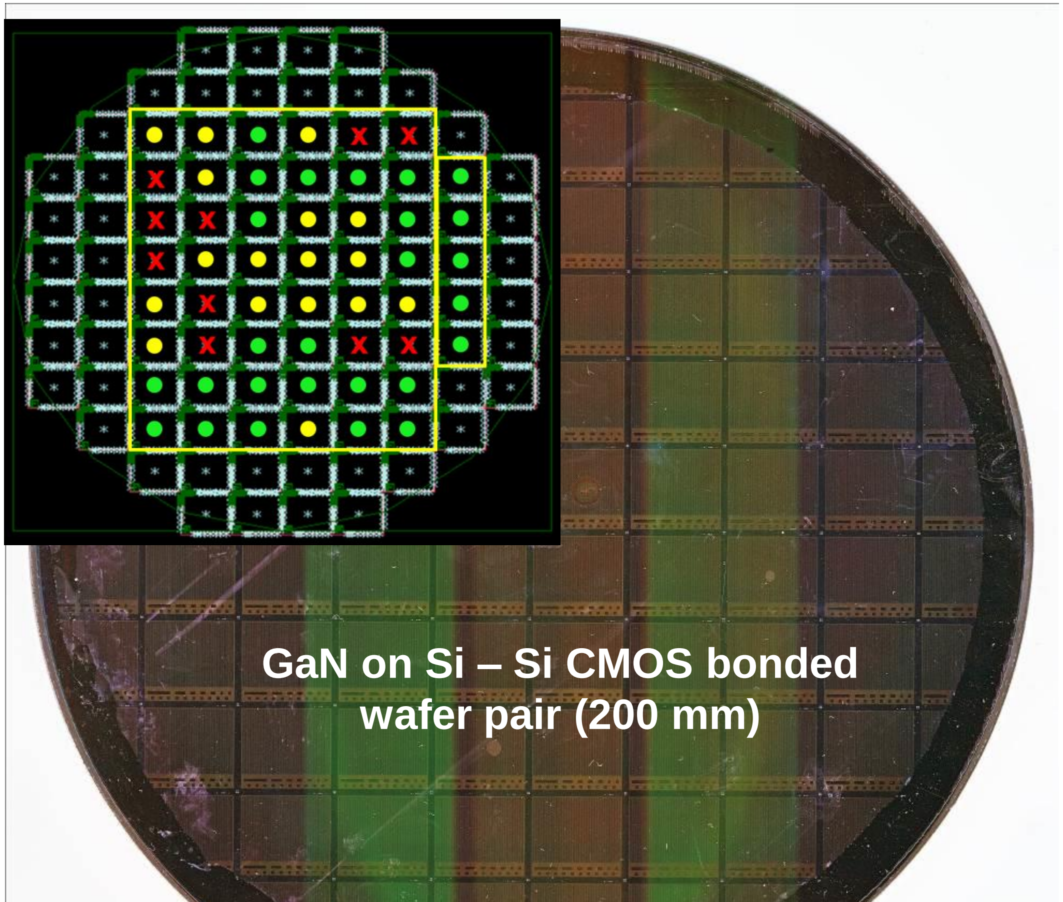


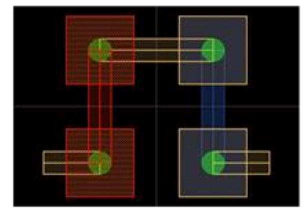


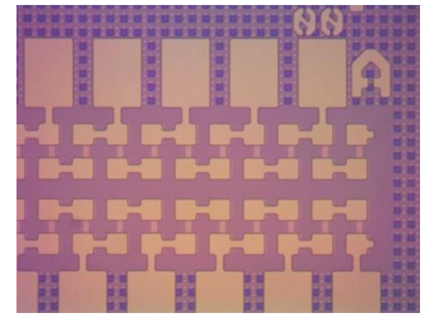
Cross Section of metallized TDVs to CMOS (E1) and GaN (M1H) layers

- **Oxide-oxide wafer bonding**
  - **Stress compensation oxide + bonding oxide = no voids**
  - **Excellent bond strength (energy > 1500 mJ/cm2)**
- **Cu filled Through Dielectric Vias (TDVs)**

GaN – Si CMOS Wafer Scale Heterogeneous Integration







Heterogeneous Interconnect 'Daisy Chain' Yield Structure

- **1024 vias per chain**
- **Each link comprises 4 vias and 4 straps**

Low-resistance and high yield Heterogeneous Interconnects across 200 mm bonded GaN-on-Si – Si CMOS wafer pairs

GaN – Si CMOS Wafer Scale Heterogeneous Integration

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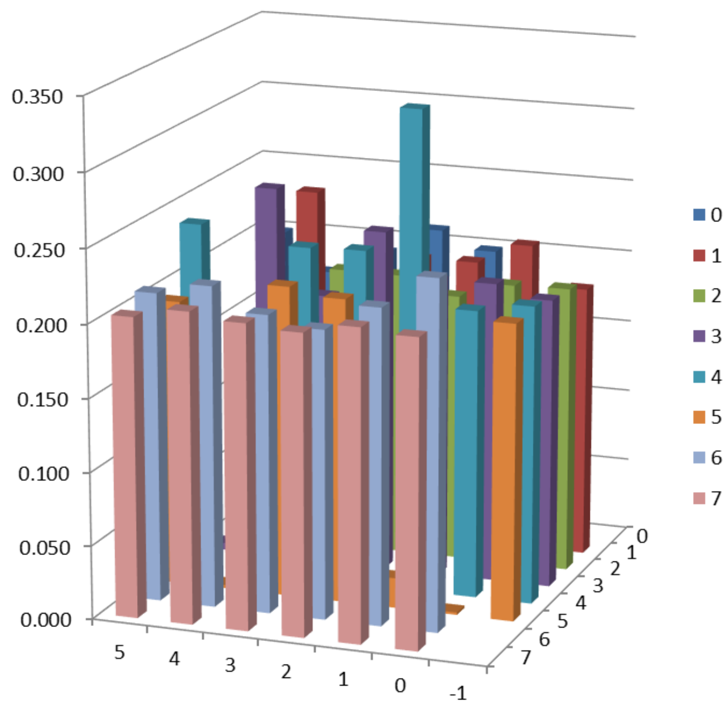

Link resistance: 0.210 +/- 0.024 Ω

Low-resistance and high yield Heterogeneous Interconnects across 200 mm bonded GaN-on-Si – Si CMOS wafer pairs

GaN – Si CMOS Wafer Scale Heterogeneous Integration RF Performance

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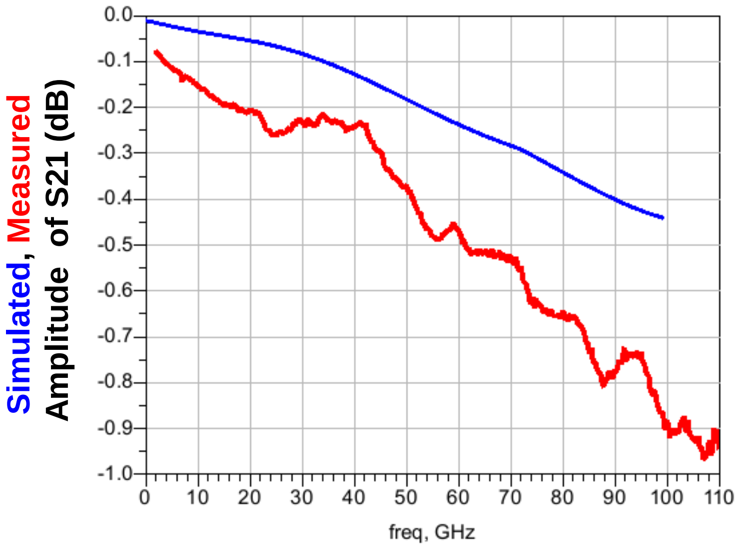
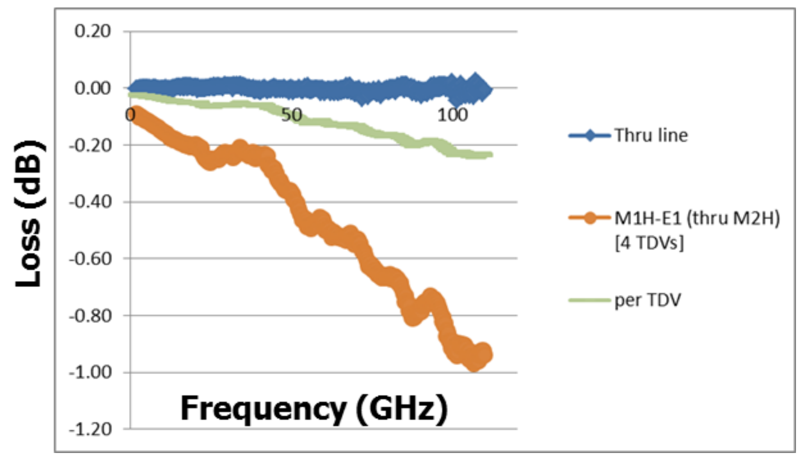
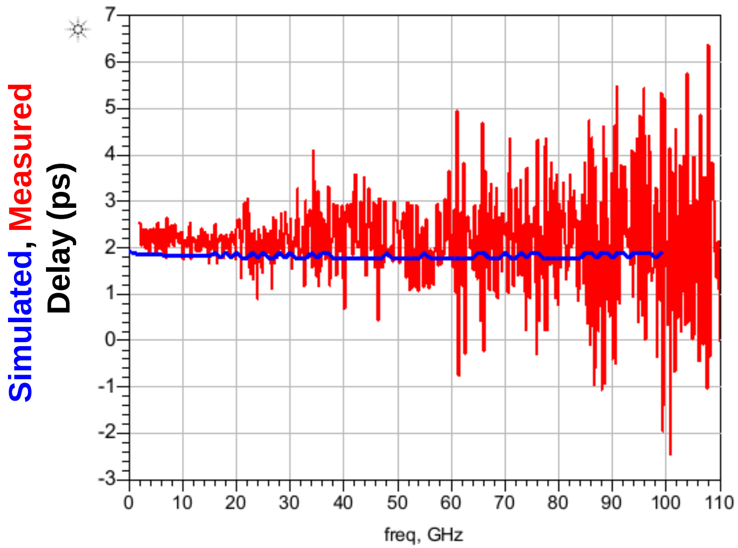


Though Dielectric Vias (TDV) Interconnects





Low-loss Heterogeneous Interconnects across 200 mm bonded GaN-on-Si – Si CMOS wafer pairs

Post Wafer bonding GaN Transistor Performance

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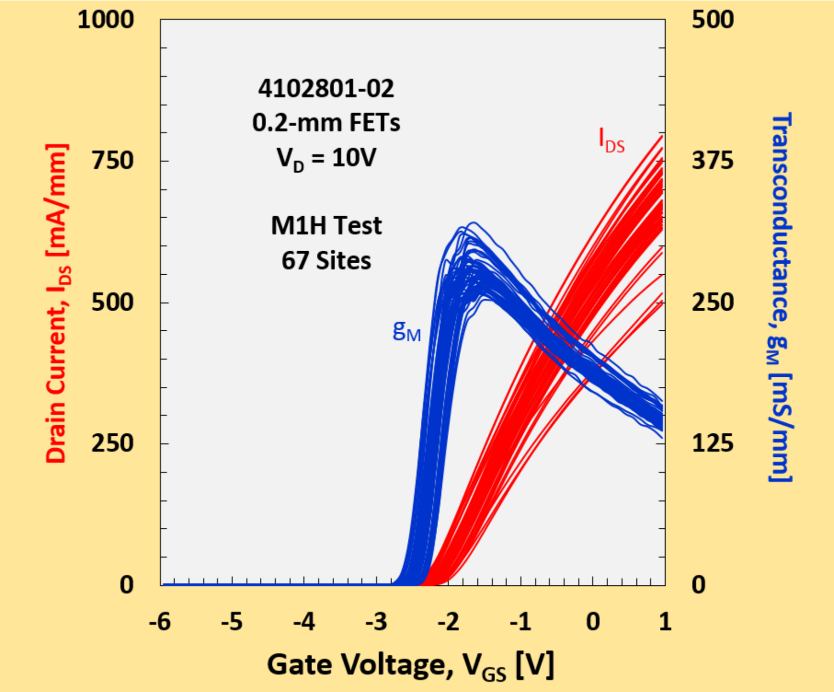
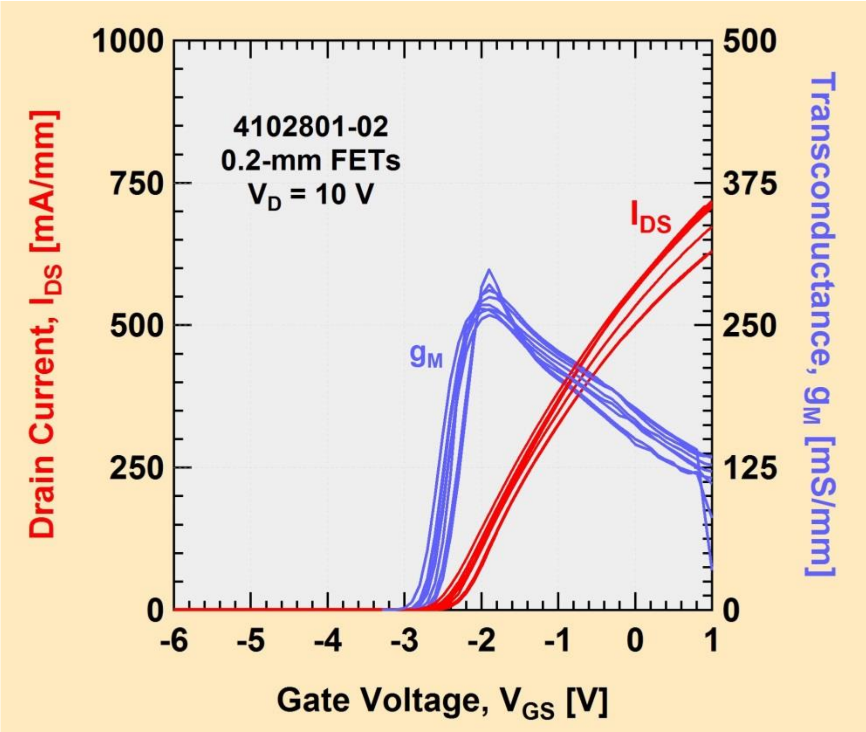


Pre-bonding DC test



Post heterogeneous integration (wafer bonding and TDV) DC test

Initial testing indicates functional GaN transistors with no change in DC and small signal RF performance after wafer bonding (heterogeneous integration)

Heterogeneous Integration: Unprecedented flexibility for advanced RF and mixed signal circuit design

- Transceiver-on-a-chip (for analog and digital beamforming arrays)
- High power digital-to-analog converters (DACs)
- Active/adaptive bias control
- Linearized, reconfigurable power amplifiers
- High dynamic range receivers/transcievers
- Active mixers
- On-wafer wireless transmitters
- Driver stages for on-wafer optoelectronics
- Power amplifiers coupled to Si linearizer circuits
- High efficiency power converter / power conditioning circuits / power distribution network
- High speed (high power) differential amplifiers
- Buffer stages for ultra-low-power electronics

Heterogeneously Integrated III-V (GaN) – Si CMOS ICs provide higher performance (power, dynamic range, noise) than Si, SiGe or III-Vs ICs

Heterogeneous Integration Example: Notional Highly Integrated Transceiver-on-a-chip

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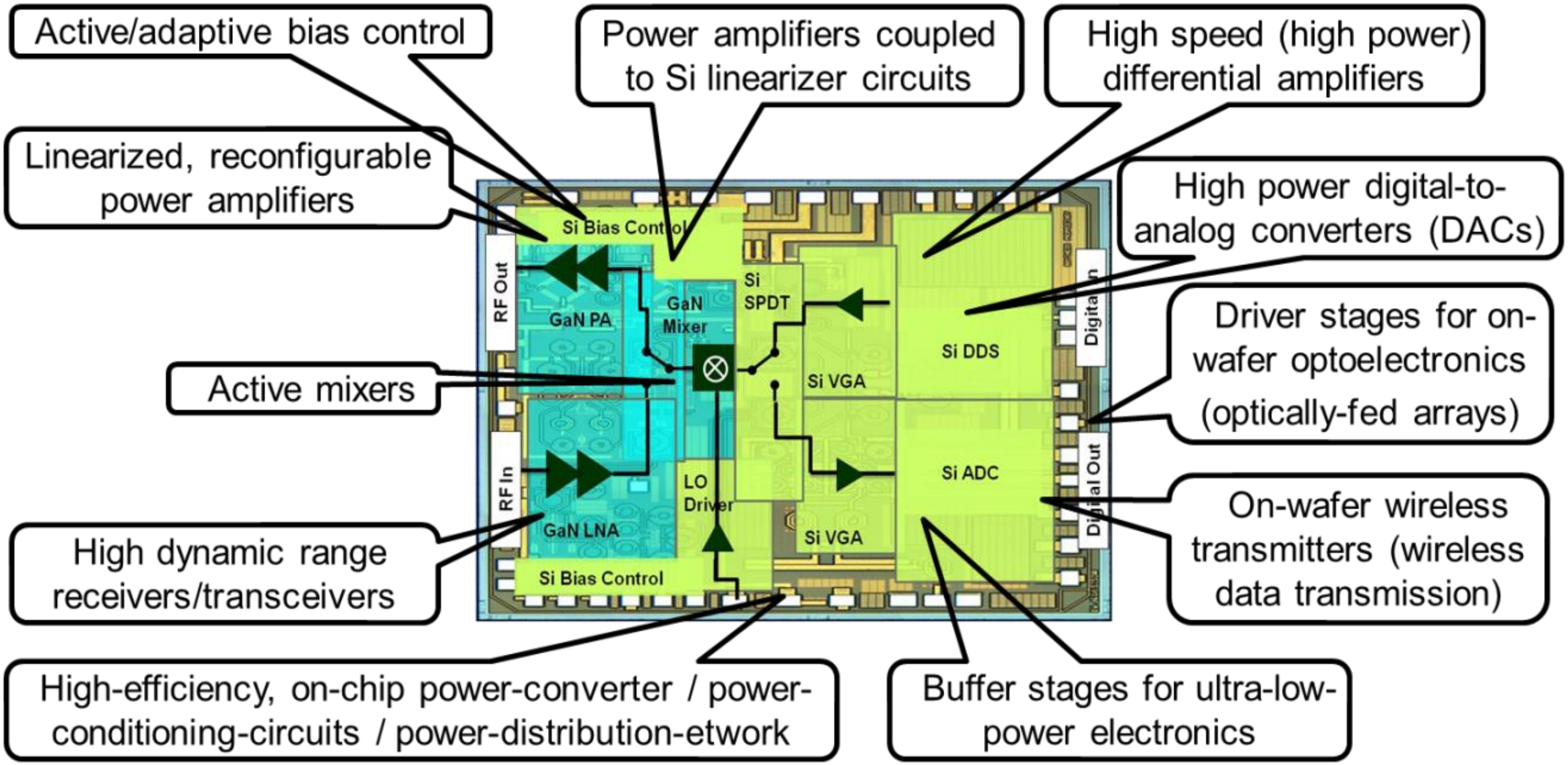

GaN/Si CMOS – SiGe BiCMOS Example Comparison

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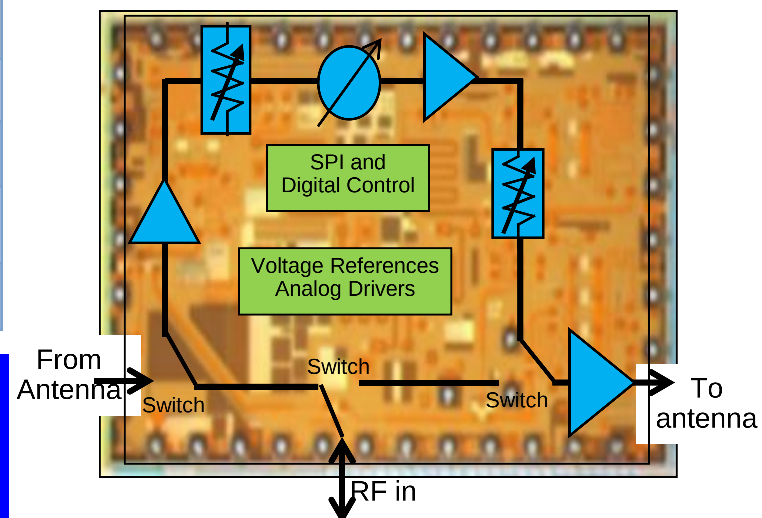
Specification	GaN – Si CMOS Transceiver (relative to SiGe Transceiver)
Frequency	X-band
Chip Size	same
Receive Noise Figure	-3dB
Input IP3	+5 dB
Rx Gain	same
Transmit P_{OUT}	+13 dB
Tx Gain	+ 5 dB
Phase Control	same
Amplitude Control	same

GaN – Si CMOS Transceiver provides higher RF performance than SiGe BiCMOS Transceiver

- **Easily and directly integrate digital interface, digital control, memory, and calibration control with RF functions on same chip**
- **Reduce latency**



Heterogeneous Integration of GaN and Si CMOS: Power DAC or Linearized Transmitter

Digital Baseband Preprocessor

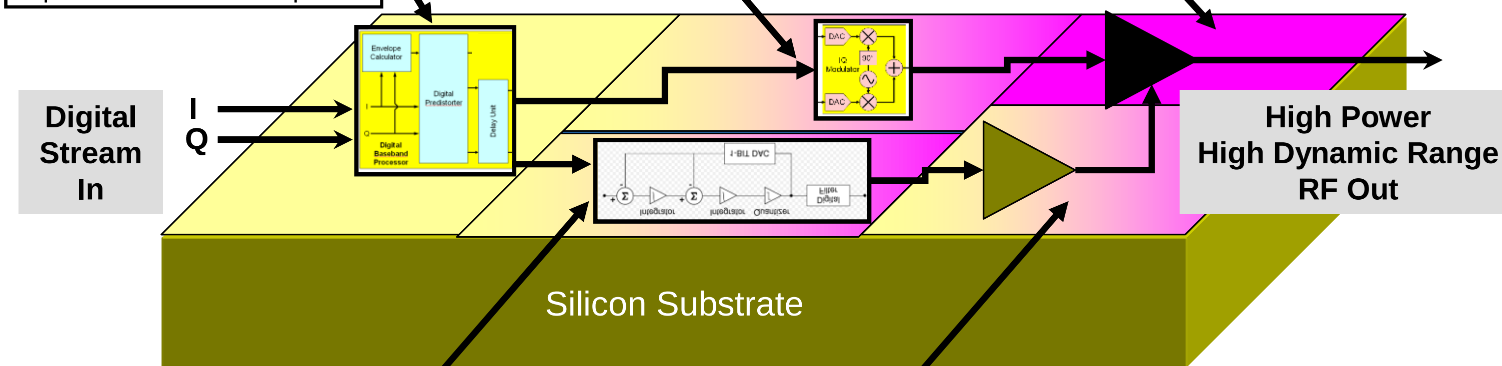
- Use silicon for digital processes
- Use knowledge of GaN transistor / HPA non-linearities to correctly derive predistortion & envelope

I/Q Modulator

- Use silicon & GaN for DAC to optimize BW / Pdc trade
- Use GaN for RF Comp.'s
- Use silicon & GaN for RF Oscillator

GaN HPA

- Use GaN Technology
- Use knowledge of device nonlinearities to achieve high efficiency
- Integrate GaN on Silicon



Δ-Σ Modulator

- Use silicon & GaN to optimize BW / Pdc trade

Class-S Modulator / Bias control

- Use silicon & GaN to optimize BW / Pdc trade

Summary

- **Heterogeneous integration**
  - **Void-free bonding GaN on Si to SOI demonstrated**
  - **Through dielectric vias (TDV) process developed**
  - **Low Loss, high yield Heterogeneous Interconnects demonstrated**
- **Repeatable device quality GaN on 200 mm Si by MBE demonstrated on multiple wafers**
  - **Good uniformity, mobility (>1600 cm^2/V-sec) and low wafer bow**
- **RF functional, Au-free GaN HEMTs on 200 mm Si wafers with Cu multilayer interconnects demonstrated at Novati on multiple lots**
  - **RF results: P_{out}: > 4.7W/mm, > 48% efficiency at 28V**

Conclusion

- Advances in materials engineering and integration are revolutionizing microelectronics
- Heterogeneous Integration of III-V (GaN) devices with Si CMOS on a common substrate has been demonstrated
- Other non-Si devices can be added to Integration Platform
- Heterogeneous Integration Enables
  - Mostly Digital High Performance RF circuits
  - Insitu control, calibration and 'health' monitoring
  - Adaptive, high efficiency, linearized PAs
  - Dynamically Reconfigurable Circuits
  - On-chip power distribution networks
  - 'Smart' power electronics
  - Sensors/Radios on a chip

Future Systems: The Marriage (Heterogeneous Integration) of Silicon, III-Vs, Passives onto a Single Chip

Questions?

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Abstract

Advances in silicon technology continue to revolutionize microelectronics. However, Si cannot do everything, particularly for high performance, high frequency RF and mixed signal applications. As a result circuits based on other materials systems, such as III-V semiconductors, are required. However, these other device technologies do not enjoy the integration density, cost benefit and manufacturing infrastructure of Si. So how can we get the 'best of both worlds'? What is the best way to integrate these dissimilar materials with Si? In this paper, we review different heterogeneous integration approaches and summarize our results on the successful wafer-scale, 3D heterogeneous integration (3DHI) of GaN HEMTs and Si CMOS.

Our Au-free GaN HEMTs have been successfully fabricated entirely in a Si foundry on semi-standard, 200 mm diameter Si wafers using Cu damascene interconnects. RF performance compares favorably with GaN on SiC devices fabricated in a III-V foundry with Au-based contact and interconnect metallurgy. Oxide bonding is being used to integrate these GaN on Si wafers with Si CMOS wafers. Through-dielectric-vias (TDVs) are used to interconnect the high performance GaN RF devices/circuits with high density CMOS control and logic circuits, resulting in ultra-short, wide-bandwidth interconnects enabling circuit optimization through intimate and arbitrary placement of CMOS logic and control circuitry relative to III-V devices. Through-substrate-vias (TSVs) are used for thermal management. This 'flexible' wafer-scale, integration platform is compatible with other III-V devices, other (non-Si) device/component technologies and any node of Si CMOS or SiGe BiCMOS. The 3DHI process is being used to fabricate cost effective, high performance, digitally enhanced, RF and mixed signal ICs such as 'intelligent' and adaptive/reconfigurable transceivers.